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EXAMINER	
ROCHE, JOHN B	

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2184	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/535,476	BRAGAGNINI ET AL.	
	Examiner	Art Unit	
	JOHN B. ROCHE	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9 and 11-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9 and 11-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 3 and 4 are objected to because of the following informalities:

2. In claim 3, line 1 "claims 1 or 2" should be -claim 1-.

3. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-9, 11 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leger et al. (US 5,781,799), hereafter referred to as Leger'799 in view of Walker et al. (US 2003/0033454), hereafter referred to as Walker'454.

6. Referring to claim 1, Leger'799 teaches a method of exchanging data within a direct memory access arrangement including a plurality of IP blocks (plurality of communication sources such as disk controllers, SCSI controllers, parallel

data ports, LANs and WANs, column 4, lines 7-9), the method comprising the steps of: associating with said IP blocks respective DMA modules (DMA controllers 20 each with multiple channels as seen in figure 1 and column 4, lines 2-3); coupling said respective DMA modules over a data transfer facility in a chain arrangement (DMA controllers 20 in a daisy chain as seen in figure 2 and column 4, lines 38-39); and associating with output buffers and input buffers coupled in a chain at least one intermediate block to control data transfer between said coupled buffers (descriptor queue 24 as seen in figure 2 and column 4, line 40).

7. Leger'799 does not teach said DMA modules each including an input buffer and an output buffer; the chain wherein each DMA module, other than the last in the chain, has its respective output buffers coupled to the input buffer of another of said DMA modules downstream in the chain and each of said DMA modules, other than the first in the chain, has its respective input buffer coupled to the output buffer of another of said DMA modules upstream in the chain; causing each of said DMA modules to interact with the respective IP block by writing data from the input buffer of the DMA module into the respective IP block and reading data from the respective IP block into the output buffer of the DMA module; and operating said input and output

buffers in such a way that: said writing of data from the input buffer of the DMA module into the respective IP block is started when the respective input buffer is at least partly filled with data, and when said reading of data from the respective IP block into the output buffer of the DMA module is completed, the data in the output buffer of the DMA module are transferred to the input buffer of the DMA module downstream in the chain or, in the case of the last DMA module in the chain, are provided as output data; controlling transfer of data between said coupled buffers over said data transfer facility by: issuing at least one request of a requesting buffer for a buffer coupled therewith to indicate at least one transfer condition selected out of the group consisting of: data existing to be transferred and enough space existing for receiving said data when transferred; issuing at least one corresponding acknowledgement towards said requesting buffer confirming that the said at least one transfer condition is met; and transferring data between said requesting buffer and said coupled buffer, whereby said data transfer facility is left free between said at least one request and said at least one acknowledgement.

8. Walker'454 teaches each DMA module including an input buffer (data is buffered internally between read and write operations, paragraph 4, lines 6-7) and an output buffer (data

is buffered internally between read and write operations, paragraph 4, lines 6-7); the chain wherein each said DMA module, other than the last in the chain, has at least one of its respective output buffers coupled to the input buffer of another of said DMA modules downstream in the chain (up to 16 possible options for connectivity, paragraph 30, lines 7-8) and each of said DMA modules, other than the first in the chain, has its respective input buffer coupled to the output buffer of another of said DMA modules upstream in the chain (up to 16 possible options for connectivity, paragraph 30, lines 7-8); causing each of said DMA modules to interact with the respective IP block by writing data from the input buffer of the DMA module into the respective IP block (writing data to destination, paragraph 4, line 3) and reading data from the respective IP block into the output buffer of the DMA module (reading data from source, paragraph 4, line 2); and operating said input and output buffers in such a way that: said writing of data from the input buffer of the DMA module into the respective IP block is started when the respective input buffer is at least partly filled with data (it is inherent to the invention that the buffer be at least partly filled with data while writing into the IP block); and when said reading of data from the respective IP block into the output buffer of the DMA module is completed, the data in

the output buffer of the DMA module are transferred to the input buffer of the DMA module downstream in the chain (couple port A to port B, paragraph 30, line 8) or, in the case of the last DMA module in the chain, are provided as output data (ports coupled to other locations, paragraph 24, lines 1-2); and controlling transfer of data between said coupled buffers over said data transfer facility by: issuing at least one request of a requesting buffer for a buffer coupled therewith to indicate at least one transfer condition selected out of the group consisting of: data existing to be transferred and enough space existing for receiving said data when transferred (DMA modules cannot function properly unless there is a method to confirm that data exists to be transferred and/or enough space exists for receiving the transferred data); issuing at least one corresponding acknowledgement towards said requesting buffer confirming that the said at least one transfer condition is met (bit 8 in transfer size configuration register set to 1, paragraph 37, line 1); and transferring data between said requesting buffer and said coupled buffer (transfer process initiated, paragraph 37, line 2), whereby said data transfer facility is left free between said at least one request and said at least one acknowledgement (read requests can still be made despite busy memory/module, paragraph 38, lines 23-25).

9. It would have been obvious to one of ordinary skill in the art at the time of invention to modify Leger'799's system to incorporate, as taught by Walker'454, said DMA modules each including an input buffer and an output buffer; the chain wherein each DMA module, other than the last in the chain, has its respective output buffers coupled to the input buffer of another of said DMA modules downstream in the chain and each of said DMA modules, other than the first in the chain, has its respective input buffer coupled to the output buffer of another of said DMA modules upstream in the chain; causing each of said DMA modules to interact with the respective IP block by writing data from the input buffer of the DMA module into the respective IP block and reading data from the respective IP block into the output buffer of the DMA module; and operating said input and output buffers in such a way that: said writing of data from the input buffer of the DMA module into the respective IP block is started when the respective input buffer is at least partly filled with data, and when said reading of data from the respective IP block into the output buffer of the DMA module is completed, the data in the output buffer of the DMA module are transferred to the input buffer of the DMA module downstream in the chain or, in the case of the last DMA module in the chain, are provided as output data; controlling transfer of data

between said coupled buffers over said data transfer facility by: issuing at least one request of a requesting buffer for a buffer coupled therewith to indicate at least one transfer condition selected out of the group consisting of: data existing to be transferred and enough space existing for receiving said data when transferred; issuing at least one corresponding acknowledgement towards said requesting buffer confirming that the said at least one transfer condition is met; and transferring data between said requesting buffer and said coupled buffer, whereby said data transfer facility is left free between said at least one request and said at least one acknowledgement. The motivation to combine these teachings is to enable other modules to access the system bus while a DMA controller is handling a transfer between two modules (paragraph 5, lines 2-6).

10. Note that claim 9 contains the corresponding limitations of claim 1 as shown above; therefore, it is rejected using the same reasoning accordingly.

11. As to claim 3, Walker'454 teaches the method of claim 1, further comprising the steps of: including a CPU in the arrangement (processor 7, paragraph 33, line 1); using said CPU for transferring data to be processed into the input buffer of the first DMA module in said chain (processor 7 issues a data

instruction to DMA controller 5 and writes the source address to the source configuration register, paragraph 33, lines 1-5); and using said CPU for collecting said output data from the output buffer of the last DMA module in said chain (processor 7 issues a data instruction to DMA controller 5 and writes the destination address to the destination configuration register, paragraph 33, lines 1-5).

12. Note that claims 5, 11 and 14-15 contain the corresponding limitations of claim 3 as shown above; therefore, they are rejected using the same reasoning accordingly.

13. As to claim 4, Walker'454 teaches the method of claim 3, further comprising the step of: configuring said DMA modules via said CPU (processor 7 issues data transfer instructions containing source address and destination address to DMA controller 5, paragraph 33, lines 1-4).

14. As to claim 6, Walker'454 teaches the apparatus of claim 5 wherein at least one of said input and output buffers has a fixed data width with respect to said data transfer facility (consistent data width regarding bus transfers is inherent to proper functionality of DMA modules) and a selectively variable data width with respect to said respective IP blocks (variable buffer size parameters bits 4:2 in source and destination configuration registers, paragraph 33, line 10 - paragraph 34).

15. Note that claim 13 contains the corresponding limitations of claim 6 as shown above; therefore, it is rejected using the same reasoning accordingly.

16. As to claim 7, Walker'454 teaches the apparatus of claim 5 or 6, further comprising: a slave interface module (processor 7, paragraph 33, line 1) configured to read from outside the apparatus data relating to at least one parameter selected from the group consisting of: a parameter indicating how many bits are available in at least one of said input buffers (size of the data block to be transferred, paragraph 36, lines 1-2); a parameter indicating how many bits are present in at least one of said input buffers (destination address register buffer size bits 4:2, paragraph 34); a parameter indicating how many bits are available for reading in at least one of said output buffers (source address bits 31:10, paragraph 33, line 10); and a parameter indicating how many bits are present in at least one of said output buffers (source address register buffer size bits 4:2, paragraph 33, line 10).

17. As to claim 8, Walker'454 teaches the apparatus of claim 5 further comprising: a reprogrammable finite state machine (state machine 6 as seen in figure 3 and paragraph 31, line 4) configured to drive operation of said apparatus by receiving data from at least one of said input buffers (data is buffered

internally between read and write operations, paragraph 4, lines 6-7), downloading data into said respective IP block corresponding to said at least one of said input buffers (write the data to the destination, paragraph 4, line 3), receiving data from said respective IP block (read the data from the source, paragraph 4, line 2), and storing data in said at least one of said output buffers (data is buffered internally between read and write operations, paragraph 4, lines 6-7).

18. As to claim 9, Walker'454 teaches the apparatus of claim 5 wherein at least one of said input buffers and output buffers is associated with a respective master block that is configured to exchange data between the associated buffer and said bus (data input/output connections as seen in figure 3 and paragraph 31, lines 2-3), said master block being configured to be coupled in a data exchange relationship to a buffer in a homologous direct memory access module (up to 16 possible options for connectivity, paragraph 30, lines 7-8) in an arrangement wherein said master block and said buffer coupled thereto are configured to: issue at least one request of a requesting buffer for a buffer coupled therewith to indicate at least one transfer condition selected out of the group consisting of data existing to be transferred and enough space existing for receiving said data when transferred; issue at least one corresponding

acknowledgement towards said requesting buffer confirming that the said at least one transfer condition is met; and transfer data between said requesting buffer and said coupled buffer, whereby said data transfer facility is left free between said at least one request and said at least one acknowledgement (it is inherent to the invention that the buffer be at least partly filled with data while writing into the IP block, as well as that the architecture can determine that the buffer has sufficient space for data to be transferred).

19. As to claim 12, Leger'799 and Walker'454 do not teach the apparatus of claim 11, wherein the plurality of DMA modules comprises three DMA modules. However, an apparatus comprising three DMA modules is simply an alternative arrangement in the art.

20. It would have been obvious to one of ordinary skill in the art at the time of invention to modify Leger'799 and Walker'454's system to incorporate, as shown above, the apparatus of claim 11, wherein the plurality of DMA modules comprises three DMA modules. The motivation to combine these teachings is to enable other modules to access the system bus while a DMA controller is handling a transfer between two modules (paragraph 5, lines 2-6).

Response to Arguments

21. Applicant's arguments with respect to claims 1, 3-9 and 11-15 have been considered but are moot in view of the new ground(s) of rejection.

22. Referring to claim 1 (and by association all claims that depend on claim 1), Examiner respectfully submits that the new grounds of rejection (Leger'799 in view of Walker'454, as shown above, render moot Applicant's arguments regarding previous grounds of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN B. ROCHE whose telephone number is (571)270-1721. The examiner can normally be reached on 8:30 am - 5:00 pm, M-F EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Henry Tsai can be reached on 571-272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JR

/Henry W.H. Tsai/
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